after forming the upper electrode

forming source and drain regions in a portion of the semiconductor substrate adjacent to a periphery of the gate insulating layer.

REMARKS

Reexamination and reconsideration of the present application are requested.

Applicants have amended claims 13, 16, 19 and 20 for clarification. Accordingly, claims 13-20 remain pending in the application.

35 U.S.C. § 112

The Examiner rejected claims 13 and 20 under 35 U.S.C. § 112 first and second paragraphs, alleging that claim 13 was not reasonably enabling and that claims 13, 16, 19 and 20 contained indefinite language. Applicants have amended claims 13, 16, 19 and 20 for clarification to address these matters. Accordingly, Applicants respectfully submit that all of the claims 13-20 now fully satisfy the requirements of 35 U.S.C. § 102.

35 U.S.C. § 102

The Examiner rejected claims 13-18 under 35 U.S.C. § 102 as allegedly being anticipated by Anderson et al. U.S. patent 5,978,207 ("Anderson"). Applicants respectfully traverse those rejections for at least the following reasons.

Among other things, the method of claim 13 includes:

"*annealing the resultant structure of steps a) through d), including completing a perovskite crystal structure of the ferroelectric layer.*"

Accordingly, in the method of claim 13, the annealing step is carried out on a resultant structure including the lower seed layer on the lower electrode, the ferroelectric layer on the lower seed layer, ***and the upper seed layer on the ferroelectric layer*** (see also page 13, lines 16-18). As explained in the specification, by annealing the ferroelectric layer together with the upper and lower seed layers, the ferroelectric layer is crystalized into a uniform and stable structure throughout the layer, preventing the undesired imprint phenomenon (see, e.g., page 13 line 19-page 14, line 2; page 16, lines 8-16; page 8, line 18-page 9, line 2; cf. page 3, lines 3-12).

Applicants respectfully submit that Anderson clearly fails to disclose such a feature. Indeed, Anderson repeatedly teaches that the ferroelectric (PZT) layer (225, 125, or 25) is annealed *prior to* depositing the upper dielectric layer (227, 127, or 27) (see, e.g., col. 7, lines 7-15; col. 12, lines 9-13; col. 8, line 64-col. 9, line 3; col. 4, lines 62-67).

Furthermore, the upper dielectric layer (227, 127, or 27) in Anderson also therefore cannot serve as an "upper seed layer" since the PZT layer has already been crystallized before the upper dielectric layer is even deposited (i.e., Anderson only teaches a lower seed layer). Thus, while Anderson does refer to the lower dielectric layers (121 or 21/23) as "seeding" the ferroelectric layer (see, e.g., col. 6, lines 17-19),

nowhere does it refer to the upper dielectric layer (227, 127, or 27) as performing any seeding function.

Therefore, for at least the foregoing reasons, it is not possible for Anderson to anticipate the invention of claim 13. Accordingly, it is respectfully requested that the rejection of claim 13 based on Anderson be withdrawn.

Claims 14-18 dependent from claim 13 are deemed to be allowable for at least similar reasons.

35 U.S.C. § 103

The Examiner rejected claims 19-20 under 35 U.S.C. § 103 as allegedly being unpatentable over Anderson in view Hsu et al. U.S. patent 6,048,738 ("Hsu"). The Examiner has cited Hsu solely for the switching element noted as missing in Anderson. However, Applicants respectfully submit that Hsu fails to cure the other defects in Anderson discussed above with respect to claim 13 from which claims 19 and 20 depend. Accordingly, it is respectfully submitted that claims 19 and 20 are patentable over any combination of Anderson and Hsu.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 13-20, and pass the application to issue. In the event that there are any outstanding matters

remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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Date: 23 July 2002

By: _____
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Version with Markings to Show Changes Made

In the Claims:

Claims 13, 16, 19 and 20 have been amended as follows.

13. (Amended) A method for fabricating a ferroelectric random access memory (FRAM) device comprising:

a) forming a lower electrode;

b) forming a lower seed layer on the lower electrode;

c) forming a ferroelectric layer on the lower seed layer;

d) forming an upper seed layer on the ferroelectric layer;

e) annealing [a structure resulting from a)-d)] the resultant structure of steps a) through d), including [making characteristics of a lower face and an upper face of the ferroelectric layer be the same and] completing a [stable] perovskite crystal structure of the ferroelectric layer; and

f) forming an upper electrode on the upper seed layer.

16. (Amended) The method according to claim 13, wherein [the] forming the upper and lower seed layers includes using a ferroelectric material having a same lattice constant [similar to] as that of a material for forming the ferroelectric layer.

19. (Amended) The method according to claim 13, further comprising, prior to [the] forming the lower electrode, forming a switching element to be electrically connected to the lower electrode.

20. (Amended) The method according to claim 13, further comprising:

before [the] forming the lower electrode

providing a semiconductor substrate; and

forming a gate insulating layer on the semiconductor substrate, and

after [the] forming the upper electrode

forming source and drain regions in a portion of the semiconductor substrate adjacent to a periphery of the gate insulating layer.